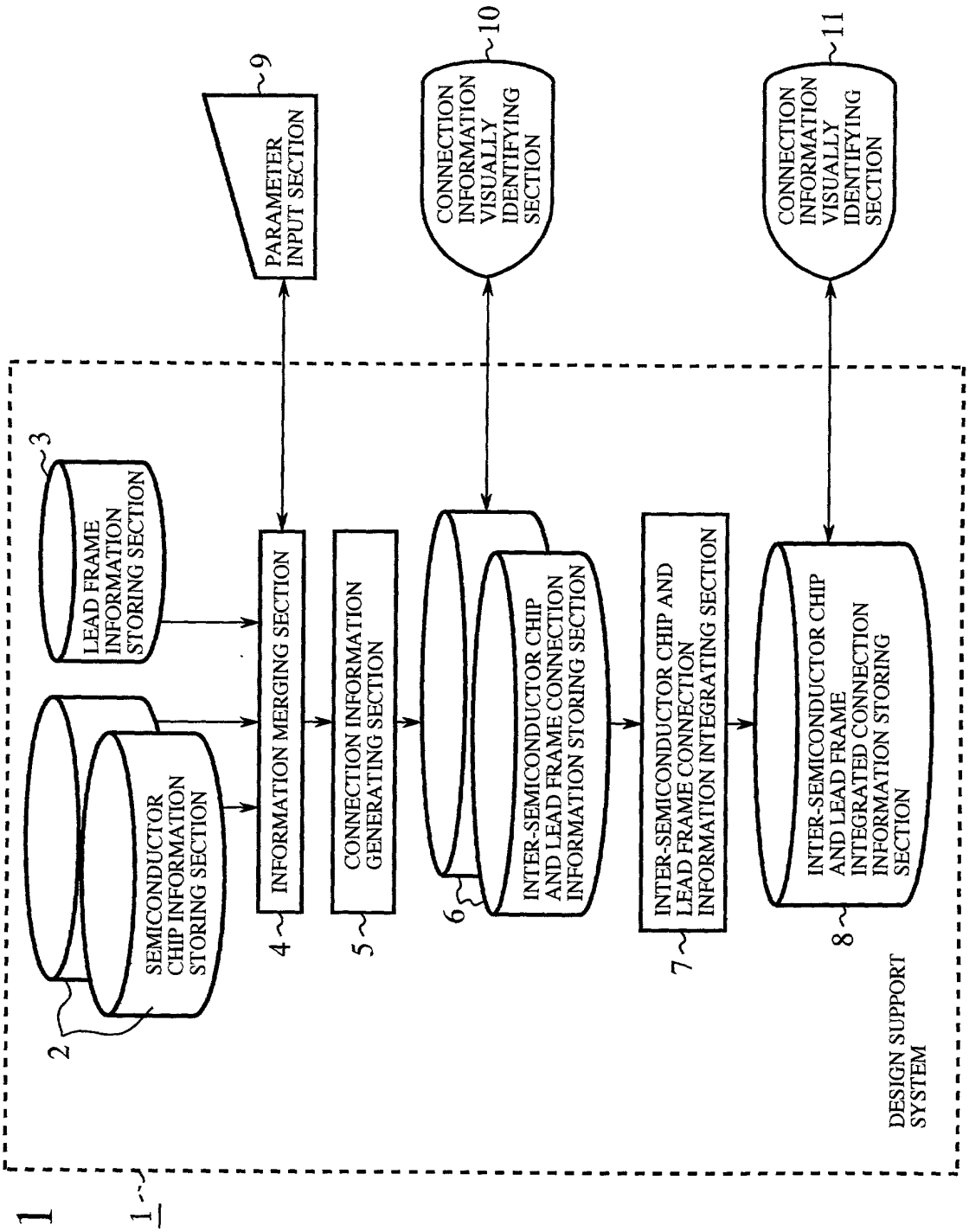
PARAMETER INPUT SECTION
9
CONNECTION INFORMATION VISUALLY IDENTIFYING SECTION
10
CONNECTION INFORMATION VISUALLY IDENTIFYING SECTION
11
LEAD FRAME INFORMATION STORING SECTION
3
SEMICONDUCTOR CHIP INFORMATION STORING SECTION
2
INFORMATION MERGING SECTION
4
CONNECTION INFORMATION GENERATING SECTION
5
INTER-SEMICONDUCTOR CHIP AND LEAD FRAME CONNECTION INFORMATION STORING SECTION
6
INTER-SEMICONDUCTOR CHIP AND LEAD FRAME CONNECTION INFORMATION INTEGRATING SECTION
7
INTER-SEMICONDUCTOR CHIP AND LEAD FRAME INTEGRATED CONNECTION INFORMATION STORING SECTION
8
DESIGN SUPPORT SYSTEM
1

FIG.1

FIG.2

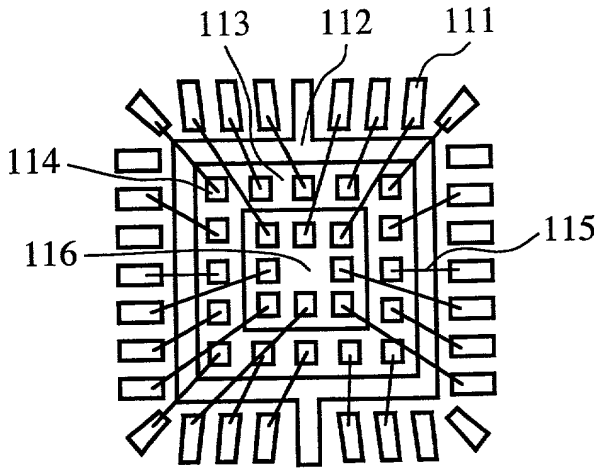

FIG.4

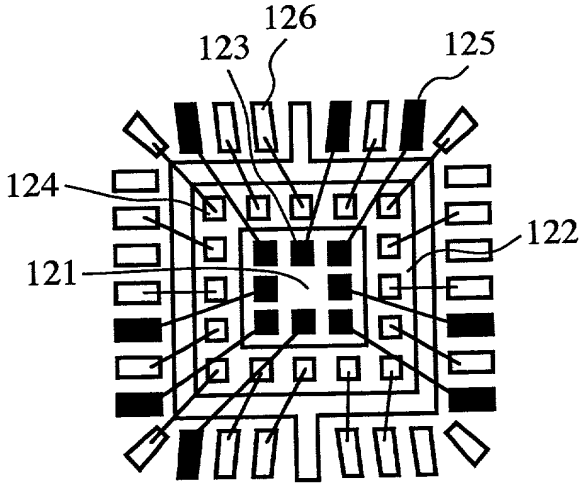

FIG.5

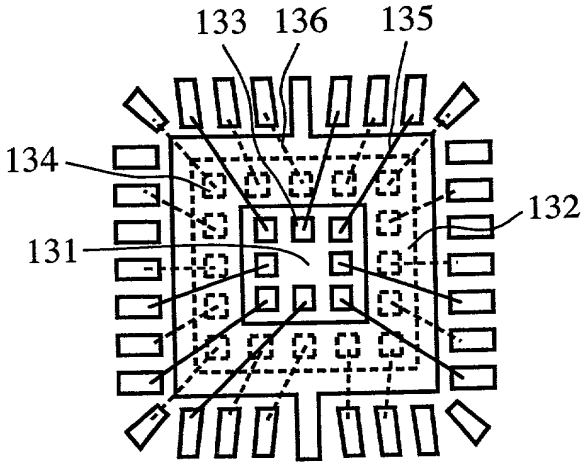

FIG.3

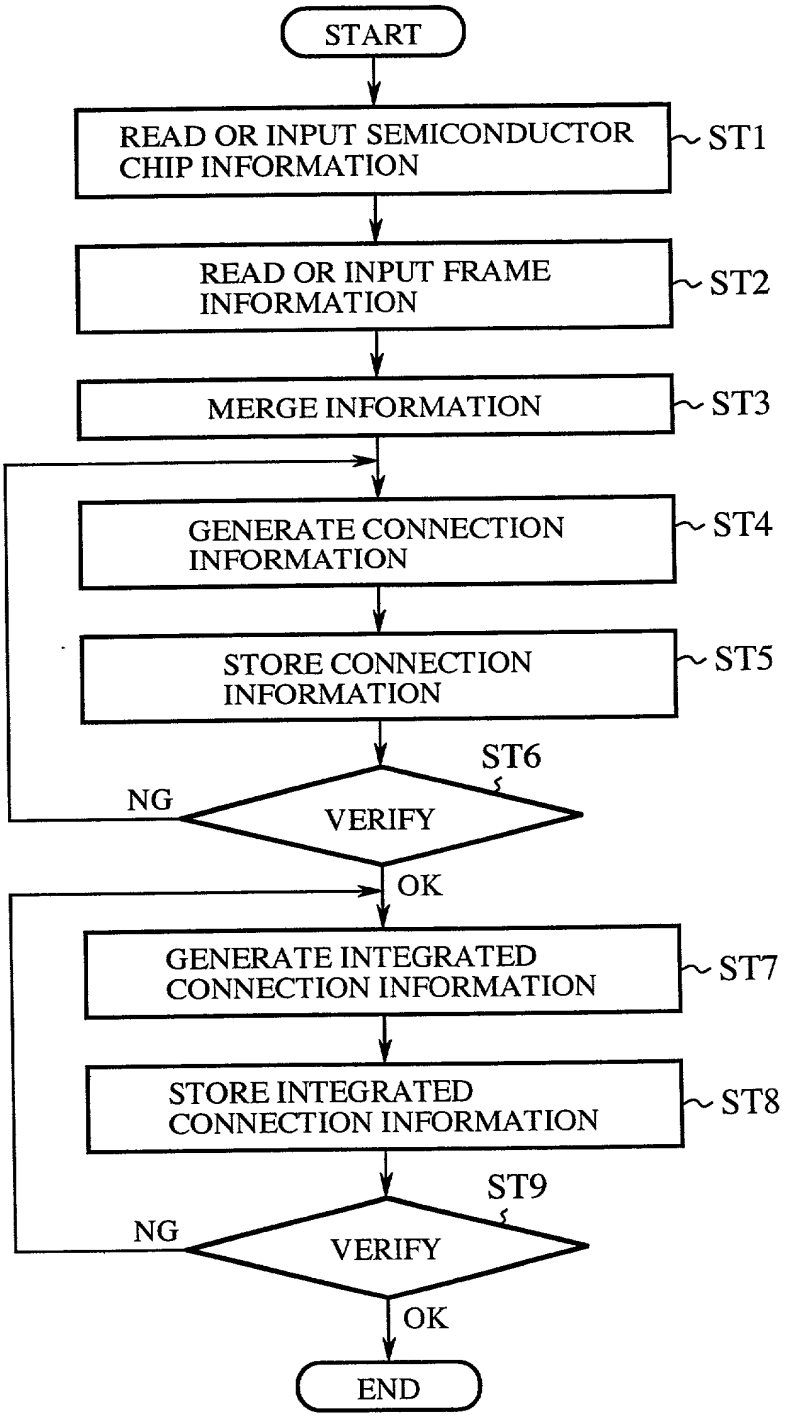
START
READ OR INPUT SEMICONDUCTOR CHIP INFORMATION
ST1
READ OR INPUT FRAME INFORMATION
ST2
MERGE INFORMATION
ST3
GENERATE CONNECTION INFORMATION
ST4
STORE CONNECTION INFORMATION
ST5
ST6
VERIFY
NG
OK
GENERATE INTEGRATED CONNECTION INFORMATION
ST7
STORE INTEGRATED CONNECTION INFORMATION
ST8
ST9
VERIFY
NG
OK
END

FIG.6

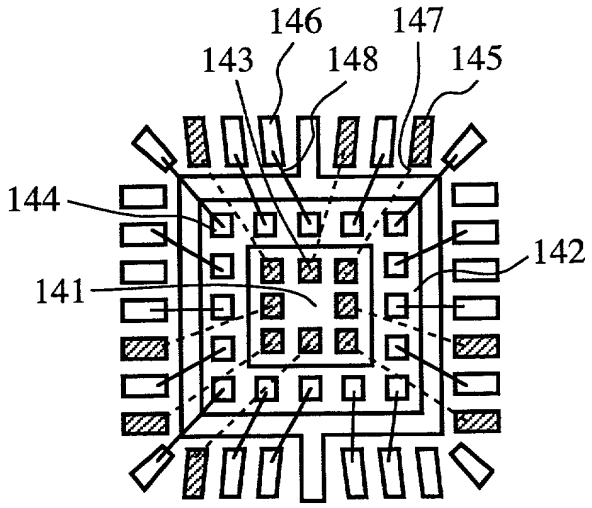

FIG.7

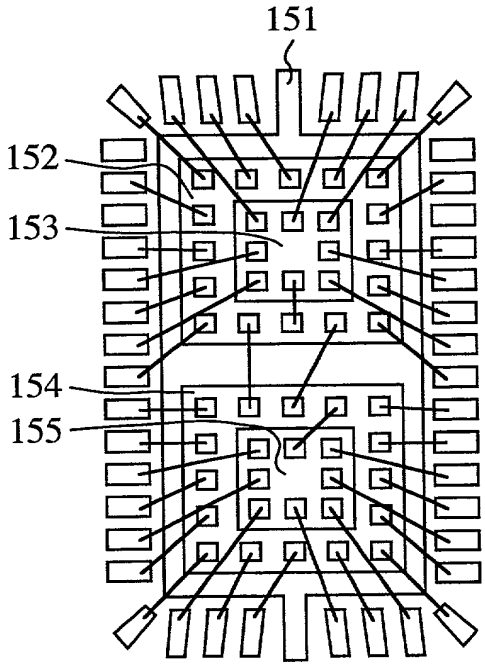

FIG.8

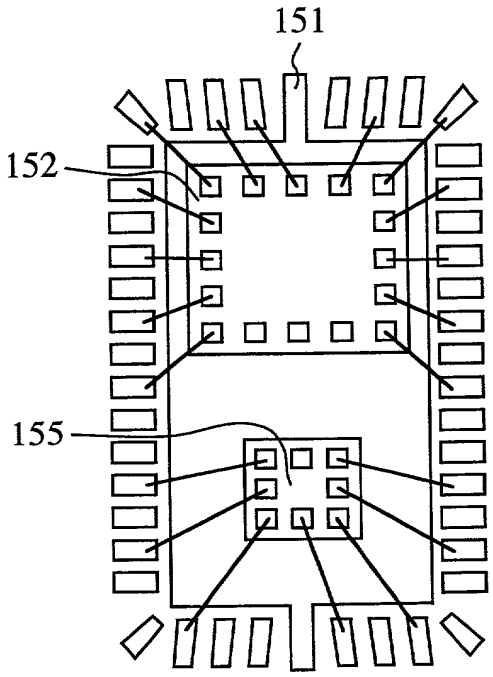

FIG.9

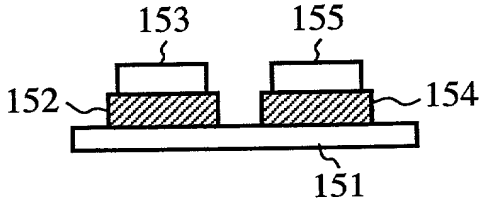

FIG.10

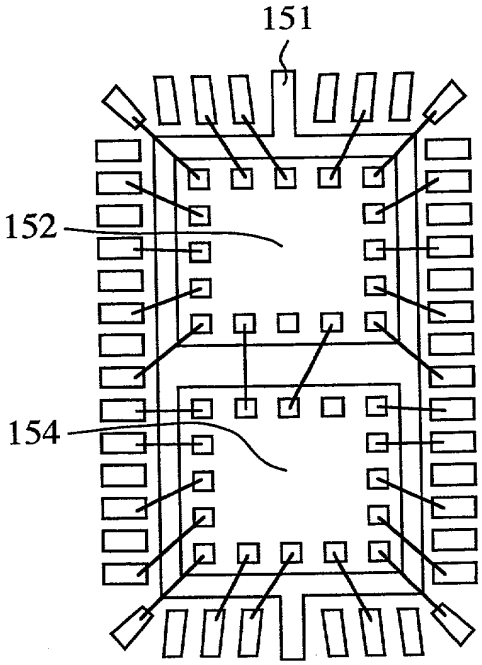

FIG.11

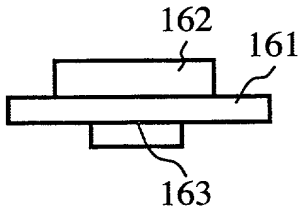

FIG.12

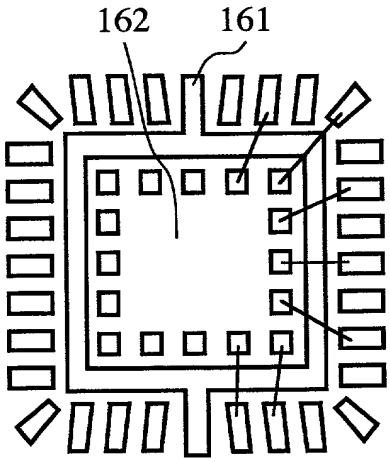

FIG.13

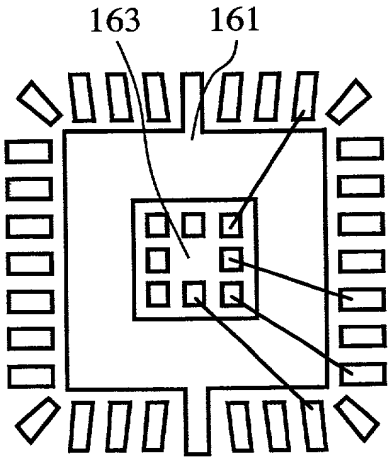

FIG.14

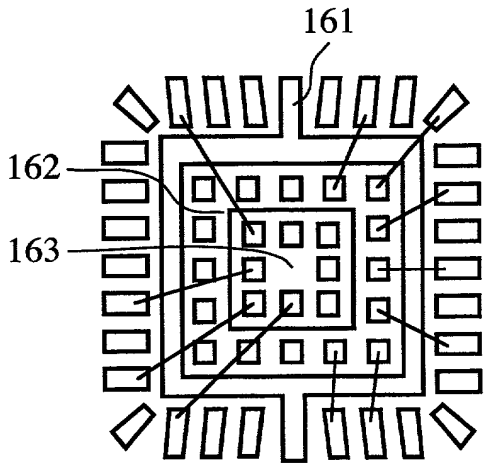

FIG.15

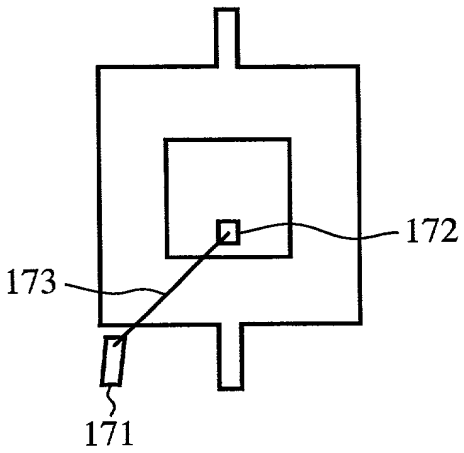

FIG.16

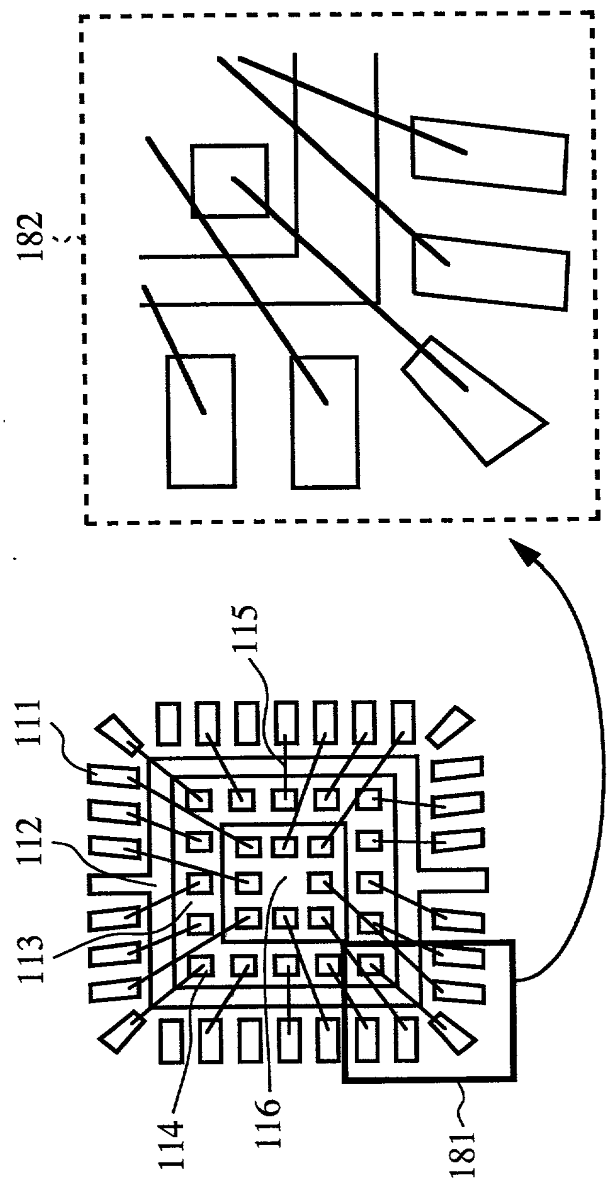

FIG.17

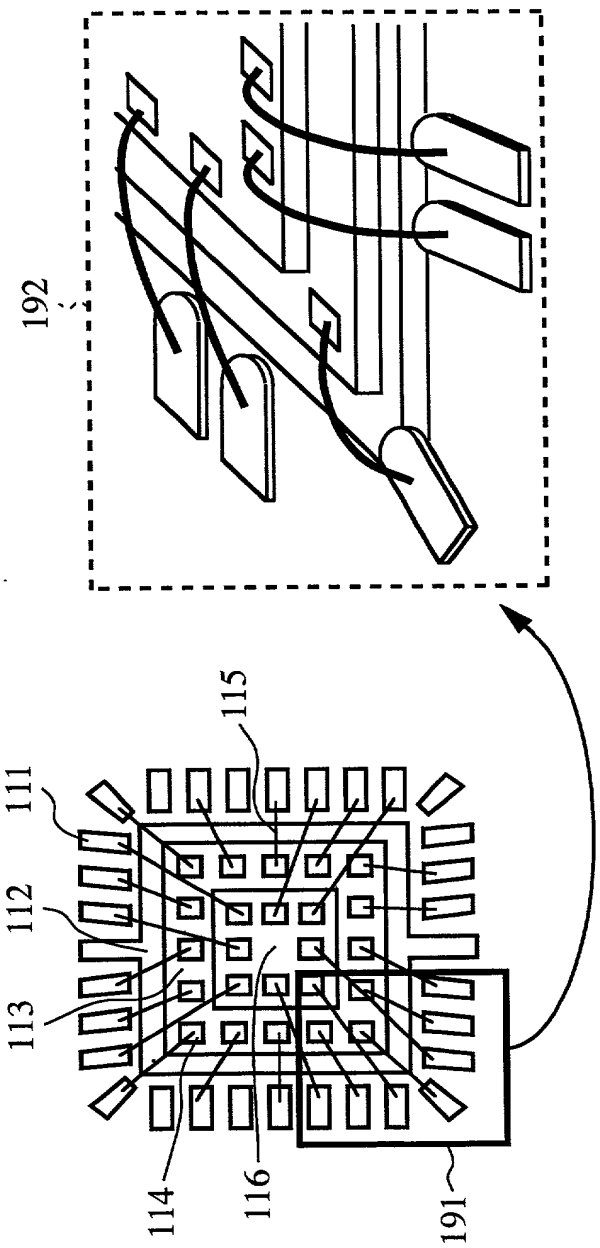

FIG.18

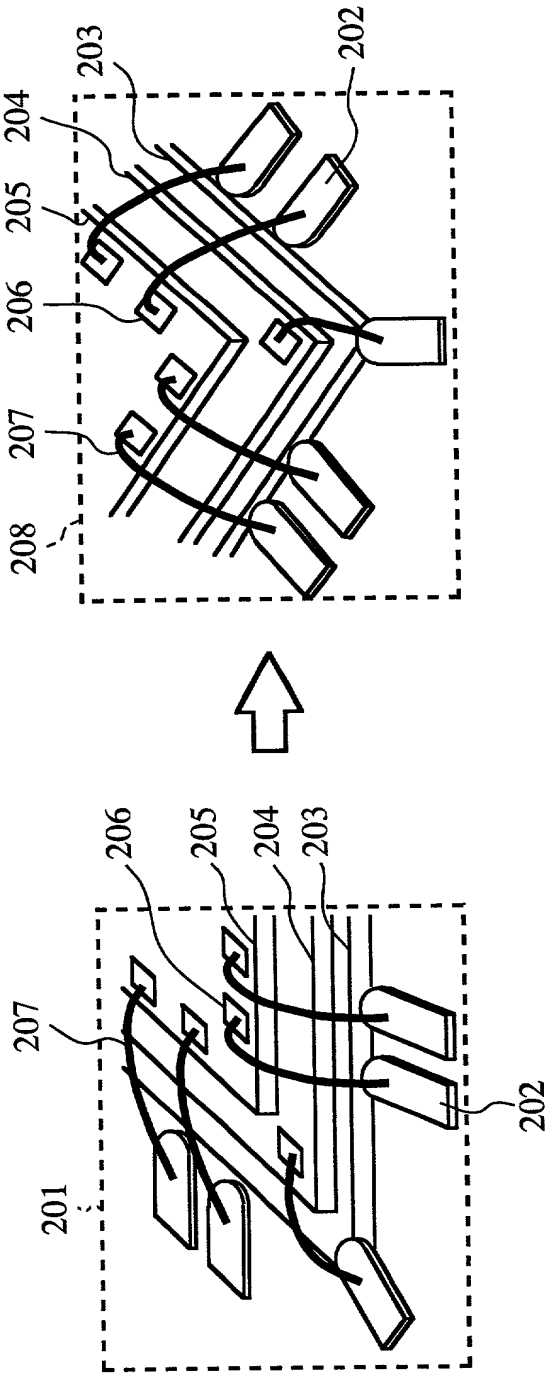

FIG.19

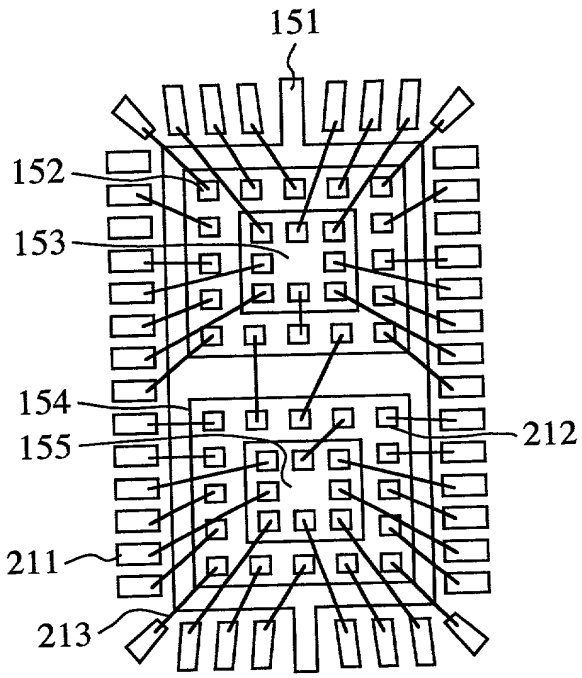

FIG.20

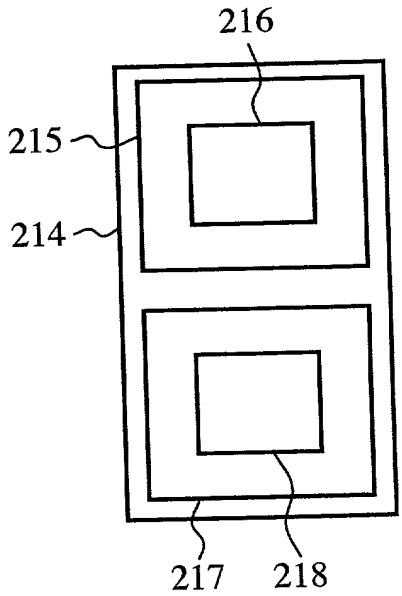

FIG.21

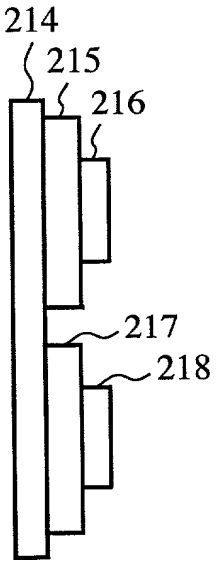

FIG.22

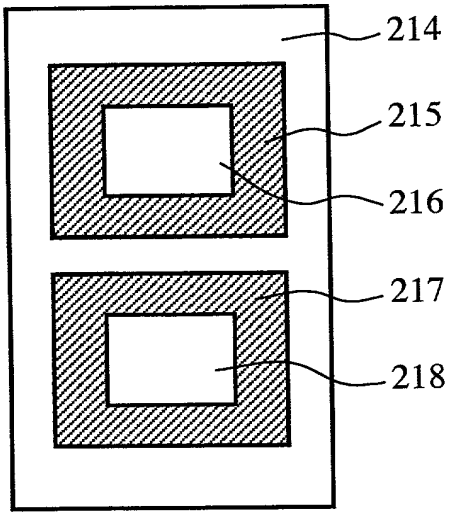

FIG.23

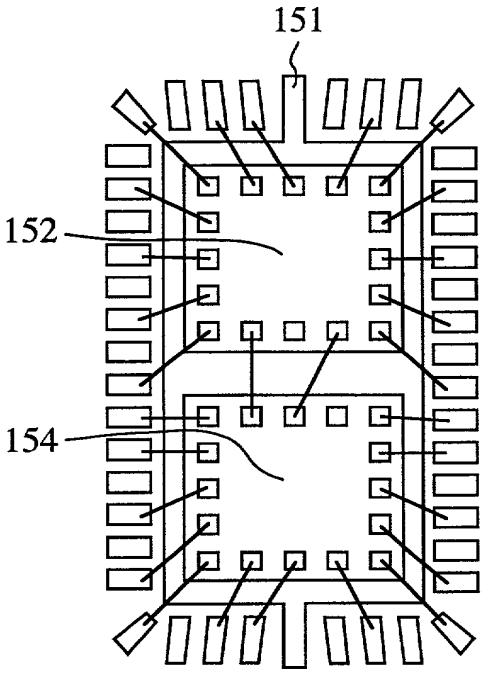

FIG.25

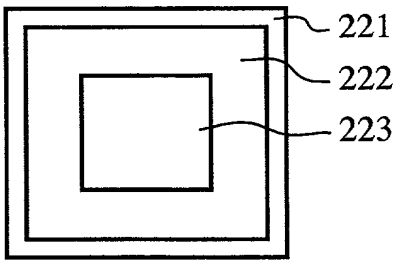

FIG.24

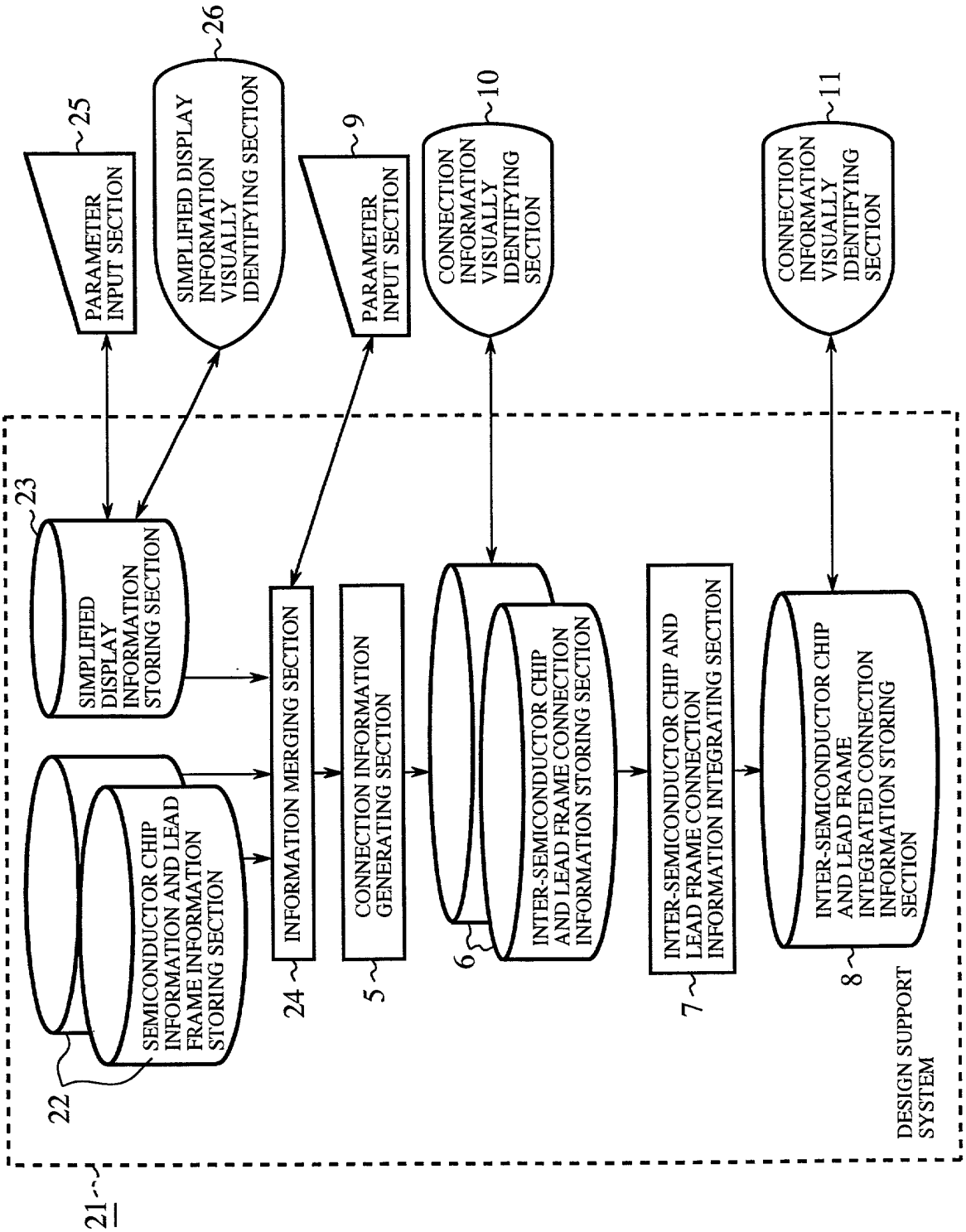

FIG.26

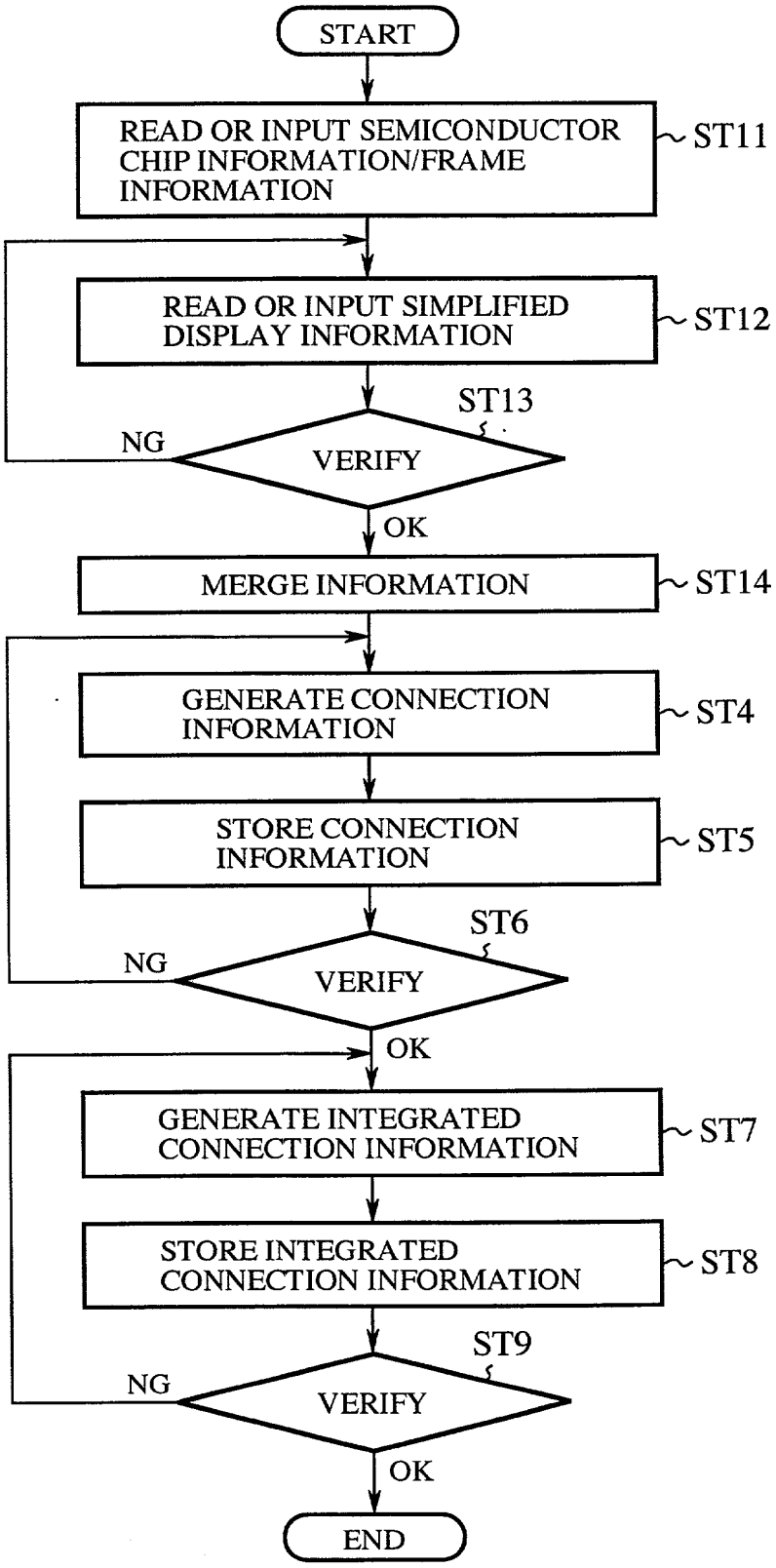
START
READ OR INPUT SEMICONDUCTOR CHIP INFORMATION/FRAME INFORMATION
ST11
READ OR INPUT SIMPLIFIED DISPLAY INFORMATION
ST12
ST13
NG
VERIFY
OK
MERGE INFORMATION
ST14
GENERATE CONNECTION INFORMATION
ST4
STORE CONNECTION INFORMATION
ST5
ST6
NG
VERIFY
OK
GENERATE INTEGRATED CONNECTION INFORMATION
ST7
STORE INTEGRATED CONNECTION INFORMATION
ST8
ST9
NG
VERIFY
OK
END

FIG.27

	FRAME	FIRST SEMICONDUCTOR CHIP	SECOND SEMICONDUCTOR CHIP
FRAME	0	16	8
FIRST SEMICONDUCTOR CHIP	16	0	0
SECOND SEMICONDUCTOR CHIP	8	0	0

FIG.28

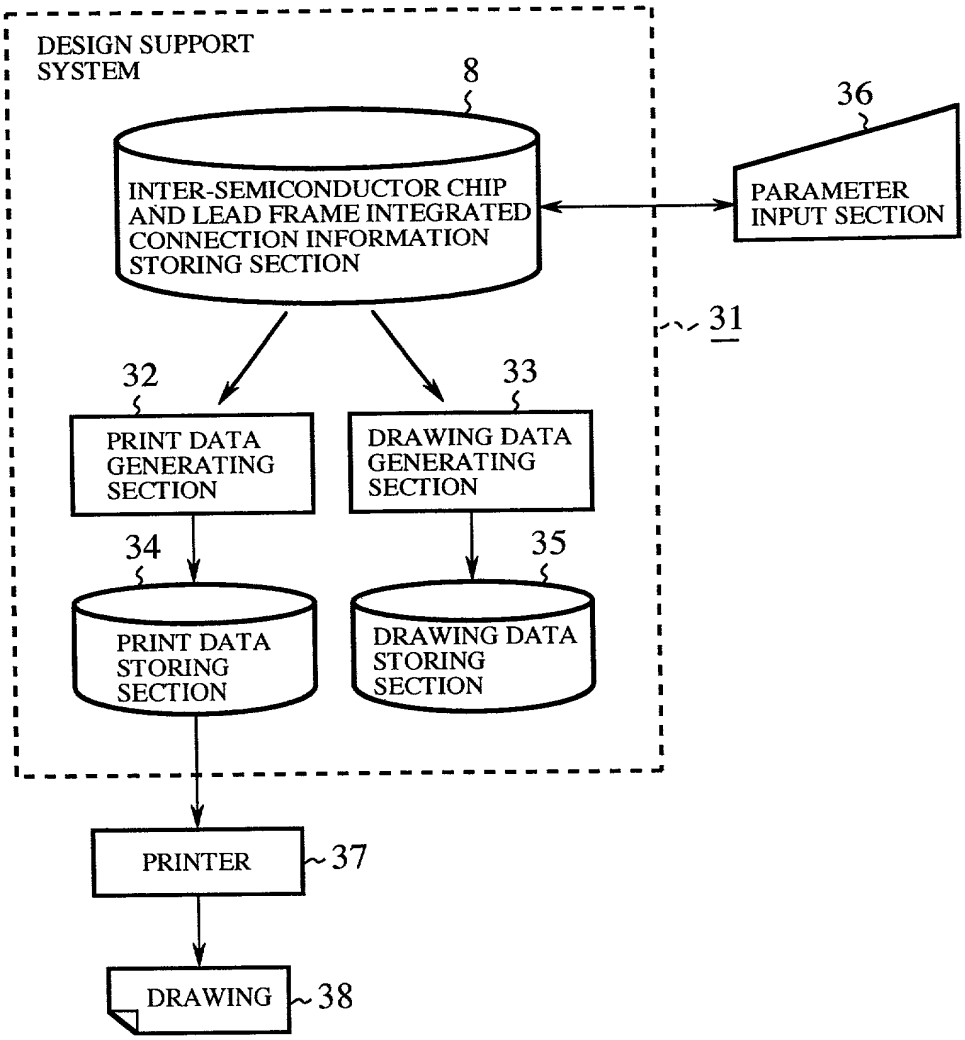

FIG.29

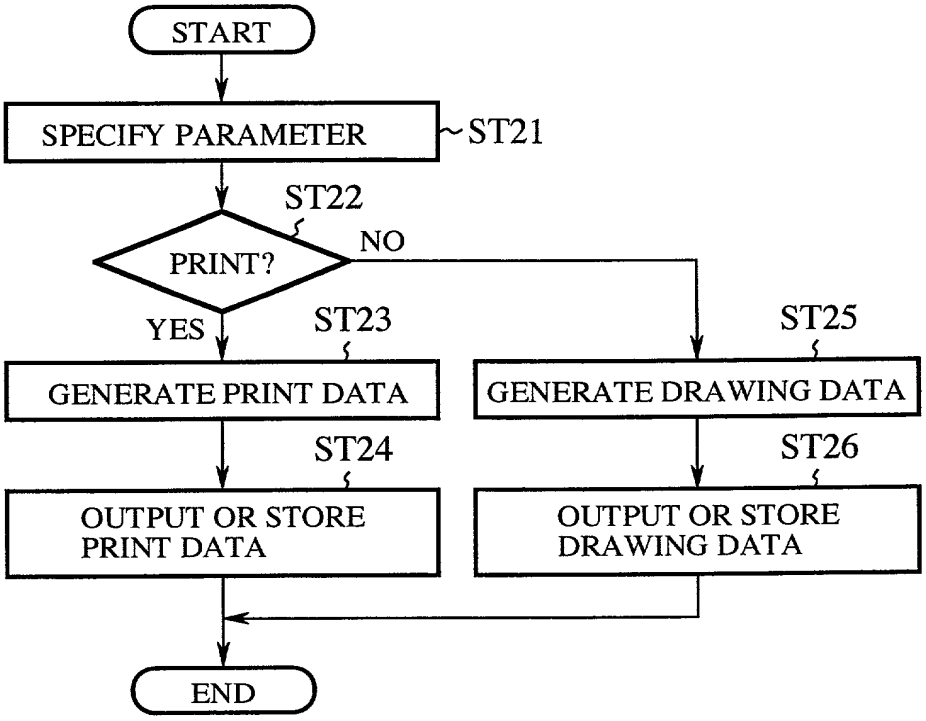

FIG.30
(PRIOR ART)

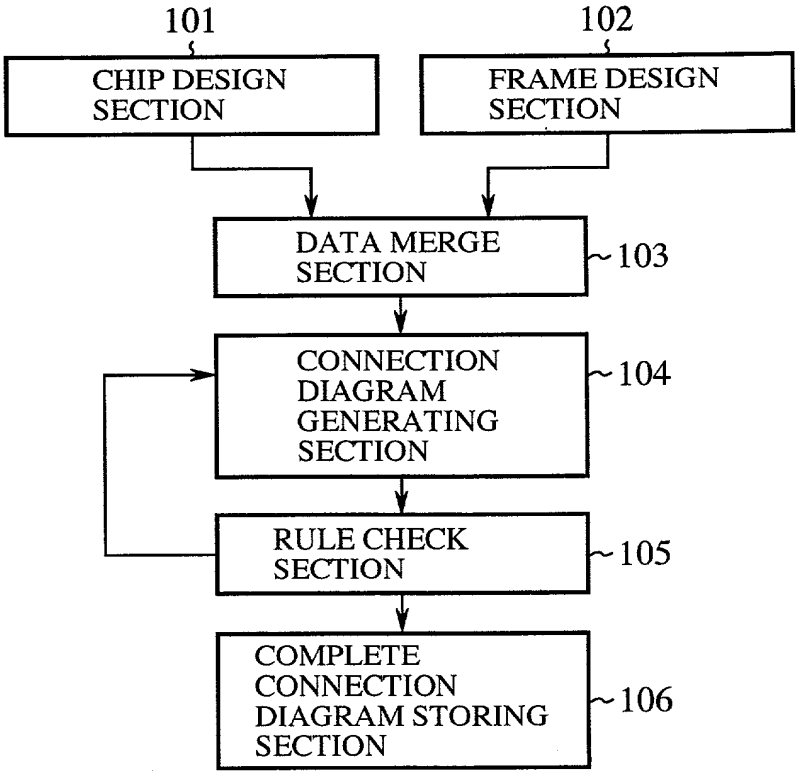

FIG.31
(PRIOR ART)

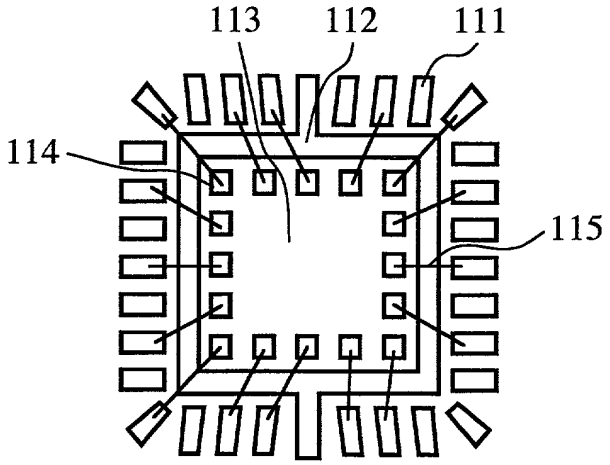

FIG.32
(PRIOR ART)